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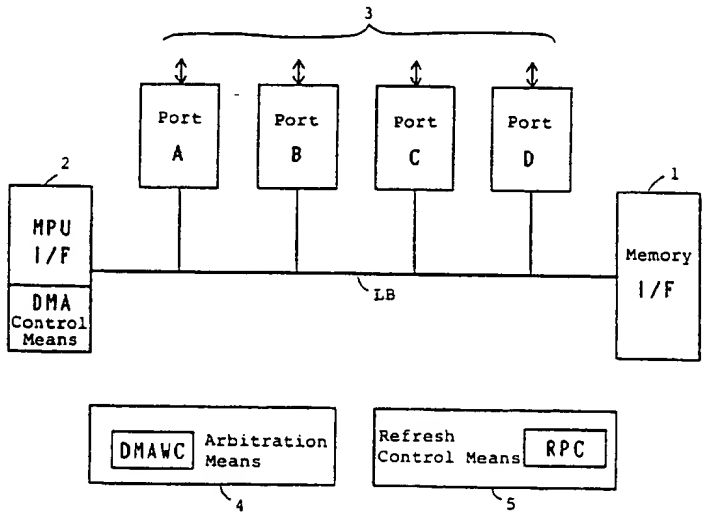
(54) Memory control device.

(57) The present invention has an object to provide a memory control device to be adapted to various demand using a standard DRAM.

This invention of a memory control device comprises a memory interface connected to a memory for outputting an address of the memory and controlling reading and writing, a plural number of input and output port connected to the memory interface through a local bus, a host interface connected to the memory interface through the local bus, a refresh control means for refreshing the memory through the memory interface, and an arbitration means for arbitrating requirements for refreshment from the refresh control means and for memory access from the input and output port and from host interface.

FIGURE 1



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FIELD OF THE INVENTION

The present invention relates to a memory control device whose standard DRAM can be used as various special memories.

BACKGROUND OF THE INVENTION

In recent years, a memory IC comes to have more various kinds of demands. There are a lot of demands for a memory IC to have multiport, many kinds of the way of accessing and scanning in addition to a lot of capacity and high speed processing. For the demand, a memory and another something to work as a memory which can access dual-port memory, field memory, orthogonal memory or the memory. possible to access the ROI (Region of Interest) are provided or proposed.

References:

(1) "Exclusive DRAM Placing Emphasis on User's Demand", Nikkei Electronics, May 2, 1988.
(2) "Exclusive DRAM is the Big Trend Involving in Standard Product", Nikkei Electronics, June 12, 1989.
(3) Mori, et al "Image Memory for Graphics Using Rectangle Area Access", The Journal of the Institute of Electronics, Information and Communication Engineers. March. 1989.
("The titles above are our translation.)

Each memory for serving such special demand has the simple function. A memory IC with multifunction does not exist. Such memory is expensive comparing to the standard DRAM.

SUMMARY OF THE INVENTION

The present invention is invented so as to solve the above problems of the prior art and has an object to provide a memory control device to be adapted to various demand using a standard DRAM.

The memory control device according to the present invention performs: i) controlling an address of a memory, also controlling reading from and writing in the memory through a memory interface, ii) data is given and received to and from outside, respectively, by the memory through a memory interface, iii) accessing to a memory in random and accessing a memory directly through host interface, iv) controlling various action with respect to the memory control device, and v) accessing to the memory in high speed through a plural number of input and output port.

It is possible to use a standard DRAM as a special memory of a multiport memory or another special memory, and easy to control.

BRIEF DESCRIPTION OF THE ATTACHED DRAWINGS

Figure 1 shows a block diagram of an embodiment of a memory control device according to the present invention.
Figure 2 shows a ground plan of the pin assignment of IC of the embodiment.
Figure 3 is a timing chart to show reading an inner register of the embodiment.
Figure 4 is a timing chart to show writing in an inner register of the embodiment.
Figure 5 is a timing chart to show the cycle of reading memory when memory is accessed in random from the host using the embodiment.
Figure 6 is a timing chart to show the cycle of writing in a memory when memory is accessed in random from the host using the embodiment.
Figure 7 is a timing chart to show cycle of reading memory when page mode access is executed on the memory from the host using the embodiment.
Figure 8 is a timing chart to show cycle of writing in a memory when page mode access is executed on the memory from the host using the embodiment.
Figure 9 is a timing chart of direct memory access with master mode using the embodiment.
Figure 10 is a timing chart to show the interruption for the host using the embodiment.
Figure 11 is a timing chart to show the output by handshake of input and output port in the embodiment.
Figure 12 is a timing chart to show the output by handshake of input and output port in the embodiment.
Figure 13 is a timing chart to show the synchronous output of the input and output port in the embodiment.
Figure 14 is a timing chart to show the synchronous input of the input and output port in the embodiment.
Figure 15 is a timing chart to show the sequential data output in image processing mode of input and output port in the embodiment.
Figure 16 is a timing chart to show the intermittent data output in image processing mode of input and output port in the embodiment.
Figure 17 shows a block diagram of an address generation mean ofs an input and output means in the embodiment.
Figure 18 show a block diagram of an input and output buffer B of an input and output port of the embodiment.
Figure 19 shows a state for memory access by

the embodiment.

PREFERRED EMBODIMENT OF THE PRESENT INVENTION

Hereinafter, an embodiment of the memory control device according to the present invention is described with reference to the attached drawings.

Figure 1 shows a block diagram of a memory control device MCD which comprises memory interface 1 connected to memory M and host interface 2 connected to a host of MPU and so force through system bus. The two interfaces are connected by local bus LB. The pin assignment of the MCD is shown in Figure 2, which is described later. In Figure 2, the codes with hyphens in the end show that they are the signals of low assert, and the numerals in the end of codes are arranged counterclockwise. In order to show the arrangement, the initial and the end of the data codes are shown inside of the device.

Connecting a plural number of the input and output port 3 to the local bus, data is timely sent and received to, or from outside and a memory interface.

The memory access between host interface 2 and input/output port 3 and the memory refresh in the refresh control means described later are controlled by mediate means 4: therefore, the interface between them is not generated.

On arbitration, considering the priority of the interfaces and ports, the interface or port with the first priority is allowed to access or refresh memory.

There are four ways for the host interface access memory: random access mode, page access mode, direct memory access with MCD master and direct memory access with MCD slave. The selection of the ways is settled beforehand in internal register of MCD (not shown).

Various internal registers are settled in order to settle a function and to store data of MCD. The address of memory M is once stored in the internal register of MCD (not shown).

For the access to the internal register, pins from AD0 to AD31 and ALT- are used. As shown in Figures 3 and 4, pins from AD0 to AD31 are used for both of internal address and data. When ALT- is low level, an address is latched and data is input and output hereafter. Reading and writing is designated by WE- (write enable) with low assert.

Pins from AD4 to AD9 are assigned for internal register address, and AD4 to AD29 are assigned for address of memory M. As the address to be designated here is word address, the memory space MCD can control is $2^{26} \times 2$ bytes, that is, 2^{27} bytes. The internal register and DRAM is selected by AD31 which is MSB of data.

In random access mode, designating the address of memory M from outside, data is read and written by 16 bits or 32 bits. Settling the length of data in the internal register, data is read and written by the predetermined cycle. Figures 5 and 6 show the read cycle and write cycle of DRAM. When the address is requested to be designated by the host, MCD samples the request of internal memory access and so forth and set RDY in low level for allowing the request of memory access of the host. After that, MCD designate low address of DRAM (12 bits) and column address (12 bits) for the memory by the 12 signal from MRCA0 to MRCA11. Address buses from AD4 to AD29 have 26 bits, by which word address of a memory is designated. The address is designated in 27 bits in total.

On page access mode, only start address is designated from outside, and column address is increased automatically by the control of DS signal from outside. The page mode of DRAM can be used as it is and memory access can be executed in high speed. Figures 7 and 8 show the reading and writing cycle on page access mode. Column address is increased by setting DS one in high level and next in low level after a column address if first generated. As ALT- is low level when the first address latch is completed, DS is changed seeing ALT-.

On direct memory access with MCD master, obtaining the right for use by MCD, data is transmitted as a bus master. Before executing the DMA, MCD outputs the signal of DMAR-. When system bus aribitration logic accept it (DMAC- is low level.), MCD has the right for use. Figure 9 shows a timing chart in the case of direct memory access with MCD master.

On writing mode on direct memory access with MCD slave, the writing address corresponding to memory M is renewed sequentially from start address by writing data on DMA data register of MCD from outside, and data is written. On the other hand on reading mode, IMC renews address automatically from start address, input the data of the memory into DMA data register, and output it sequentially.

With respect to the DMA above, it is possible to access the memory of ROI. It is possible to read and write from, or to a rectangle memory area with start address as a corner by registering the number of pixels of a necessary area, the number of rasters and offset (the number of pixels from the last raster pixels to the start pixel of the next raster) in the inner register beforehand. The memory access of DMA is settled rather lower priority. The weight counter of DMA "DMAWC" is increased every time when access request is not accepted in the predetermined time. DMA is given higher priority according to the counted value as an indication, and

the count is reset when the memory access request is accepted. MCD shows the completion of DMA transmission and the completion of transmission in the input and output port described later by setting interruption signal INTR-low level as shown in Figure 10. Which port has completed transmission is shown in status register of the inner register.

MCD comprises refreshment control means 5 (shown in Figure 1) for controlling refreshment of memory M, which refreshes memory M necessarily and sufficiently accepting memory access to the utmost. For controlling it, refreshment pending counter RPC is comprised in refreshment control means 5. The number of the counter RPC is increased when refreshment is required and it is not accepted. The priority of the refreshment is made higher according to the indication of the counted number. When once refreshment is accepted, the number is decreased.

The aforementioned input and output port 3 is the set of 4 from A to D. A, B and C give and receive data to, or from outside by two-way data bus, and work independently. Port C is used as an input-only port of an image processing mode described below, or as an input port of the control signal of ports A, B and C. These ports comprise 3 kinds of data transmission modes. The role of each port is settled beforehand in an image processing mode (described later) in the 3 kinds of modes. The 3 data transmission modes of port 3 is a handshake mode, a synchronous mode and in image processing mode.

On these transmission, MCD can perform simultaneously expansion, contraction, reverse change of direction of scanning for reading and execution change into non-interlace from interlace.

Settlement of transmission mode and other function is recorded in an inner register

Figures 11 and 12 shows timing charts of output and input of handshake mode. ARDY signal and AVLD- signal are used for the handshake. On outputting, when ARDY signal is made high level from outside, MCD outputs data from PA0 to PA7 as soon as the data is prepared to be output, simultaneously, it makes AVLD- signal low level. AVLD- signal shows the efficiency of data. On inputting, when ARDY signal is high level, it is possible to input data. When data is input from outside and AVLD- signal is low level, the data is latched. Here in figures, the signal name (pin assignment) of port A is representatively shown: concerning to other ports, the signals substituted B, C and D for A are used.

Figures 13 and 14 show timing charts of input and output in synchronous mode. Data is input and output synchronously with SCLK. When ARDY signal is mode high level from outside, MCD outputs data from PA0 to PA7 as soon as the data is prepared to be output, simultaneously, it makes AVLD- signal low level. AVLD-signal shows the efficiency of data here, too. When ARDY signal is high level, data can be input. When data is input from outside and AVLD- signal is low level in the state that ARDY signal is high level, the data is latched.

On image processing mode, ports from A to C are used for output ports and port D is used for input port. YLOAD us used for the starting signal of 1 plane (the signal is corresponding to the vertical blank of indication system), XLOAD is used for the starting signal of 1 raster (it is corresponding to the horizontal blank of indication system), MODEOUT is used for pipeline control signal of an image processing system. They are shown in Figures 15 and 16. The data to be processed is input from a memory and sent to an image processing system from ports A, B and C. The result through the image processing system is input to port D and stored in a memory. Signal MODEIN shows the effectiveness and ineffectiveness of output data of the image processing system, which can be input to MCD. Signal RSTR- is a timing signal for sequential processing of the image processing system, which refresh the line memory for storing the previous raster before starting raster scan. This refreshment is executed with a little delay from the rising of XLOAD. Figure 15 shows an example that transmission of an image of 1 plane is executed sequentially. Figure 16 shows an example that data transmission is interrupted by making MODEOUT low level for the refreshment of memory M.

The address generation means of aforementioned input and output port and host interface is structured as in Figure 17. It comprises an address register ADR for generating address for a memory, a line number register LNR for registering the number of rasters in vertical direction of the area to be accessed, pixel number register PNR for registering the number of pixels in horizontal direction of the same area, and offset register OSR for registering the change of the coordinates with respect to horizontal direction on the movement of location for access from one raster to be next raster. PNR is connected to pixel counter PC. PC loads the data of PNR just before the access to a raster, and decrease the counted number every time accessing data corresponding to a pixel. LNR is connected to line counter LC. LC loads the data of LNR just before the access to rectangle area, and decrease the counted number every time completing 1 raster of access. It it possible to designate the end points of a raster and of the area on access to the rectangle area above by these steps. When an access to a memory is started, start address is registered in address register APR. The

address number is increased by increment signal INC. The memory address to make an access is calculated appropriately according to the data of LC and PC. The address value is output from MRCA0 to MRCA11 after it is given to address register ADR. The coordinates in vertical direction of an image is increased every time 1 raster is completed. The coordinates in horizontal direction of an image is increased on 1 raster, but when the coordinates come to the end point, the first horizontal address of the next raster is decided by the addition of the value of ADR and OSR by adder ADD. Executing it, the start address of the next raster can be generated in high speed.

The above is the description with respect to the forward scanning. The backward scanning is describe later.

The one adder is commonly used as the address generation means of each port. A gate of a circuit is efficiently used by it.

As the address generation means above is independently set by every port, an address can be set perfectly independent of other address settlement. When input and output of some ports are defined for a memory, the function of a multiport memory can be obtained. For example as shown in Figure 19, the area of a memory A and B can be made access by both of ports A and B.

In addition to such usual address generation, it is possible to perform contraction, reverse direction scanning, transformation from interlace to non-interlace and from non-interlace to interlace.

Expansion in horizontal direction is executed by writing 1 pixel which is read out a plural number of times, and that in vertical direction is executed by writing the same raster a plural number of times.

Contraction in horizontal direction is executed by reading pixels intermittently, and that in vertical direction is executed by reading rasters intermittently.

Reverse direction scanning is executed by inputting decrement signal instead of increment signal so as to the order of generation of address is reversed.

Transformation from interlace to non-interlace and that from non-interlace to interlace are executed by i) regarding the offset on writing as the number of pixels of 1 raster, it is input by every other raster, ii) the image is input on a vacant raster in the next frame.

Input and output buffer B is settled in each port in order to input and output memory data to, and from input and output port 3 as shown in Figure 18. Buffer B comprises the first buffer BUF1 which is connected to input side of memory interface and the second buffer which is settled by following BUF1. Buffer BUF1 is a buffer with 64 bits for storing data of 64 bits output from a memory. When 64 bits data is input to BUF1, the data is immediately transmitted to BUF2. Consequently, reading of 128 bits is sequentially executed, which means that it is possible to input data in high speed. Input and output register IOR is connected on output side of buffer BUF2 through multiplexer MUX2. MUX2 input data to a port. Alternatively, it output data to BUF2.

When output of a memory is output from a port, MUX2 input the output of BUF2 to IOR. IOR outputs data 64 bits by 8 bits in parallel and input them to multiplexer MUX4. Address signal ADS is already input to MUX4. MUX4 selects 8 bits data from 1 line from the outputs of IOR and selects all the 8 bits or only 1 bit from the 8 bits data. The selected data is output from a port. In this way, the data of a memory can be output to a port by 1 bit. The input to a port is input to multiplexer MUX2. Then the input is transmitted to a memory, MUX 2 selects the outputs of MUX5 and input it to IOR. The data of IOR is transmitted to a memory from BUF2 through from MUX3 to BUF1. The data of BUF1 is immediately transmitted to BUF2 also on this data input, and memory is written by 128 bits. Therefore it is possible to input data in high speed.

The memory control device according to the present invention performs: i) controlling an address of a memory, also controlling reading from and writing in the memory through a memory interface, ii) data is given and received to and from outside, respectively, by the memory through a memory interface, iii) accessing to a memory in random and accessing a memory directly through host interface, iv) controlling various action with respect to the memory control device, and v) accessing to the memory in high speed through a plural number of input and output port. Therefore, standard DRAM can be used for a multiport memory and other special memory, and it is easy to control it.

Claims

1. A memory control device comprising:

   a memory interface connected to a memory for outputting an address of said memory and controlling reading and writing;

   a plural number of input and output port connected to said memory interface through a local bus;

   a host interface connected to said memory interface through said local bus;

   a refresh control means for refreshing said memory through said memory interface; and

   an arbitration means for arbitrating requirements for refreshment from said refresh control means and for memory access from said input

and output port and from host interface.

2. A memory control device claimed in claim 1, whose input and output port and host interface comprise:

a start address register for registering a start address for accessing to said memory:

a size register for registering size of a rectangle area for accessing to said memory;

an offset register for registering an offset of a column address on moving from low address access to the next low address access;

an addition means for adding said offset to the column address on completing said accessing of low address in said rectangle area.

3. A memory control device claimed in claim 1, wherein an input and output port comprises an input and output buffer means for temporarily storing input and output data.

4. A memory control device claimed in claim 1, whose input and output buffer means comprises the first buffer for storing data output from said memory, the second buffer for storing data to input said memory and the third buffer for storing input and output data, wherein an output of the fist buffer is connected to the input of the second buffer and an output of the second buffer is connected to the input of the third buffer through switching means which outputs an input for an input and output port and an output from the second buffer, alternatively.

5. A memory control device claimed in claim 1, whose third buffer is comprised of register groups for storing but strings of 1 byte, wherein a byte selection means for selecting one of these registers is connected to an output of the third buffer.

6. A memory control device claimed in claim 5, wherein a bit selection means is settled for outputting 1 bit selectively from a register.

7. A memory control device claimed in claim 2, wherein said addition means for an input and output port is comprised of one input and output port common to all the input and output ports.

FIGURE 1

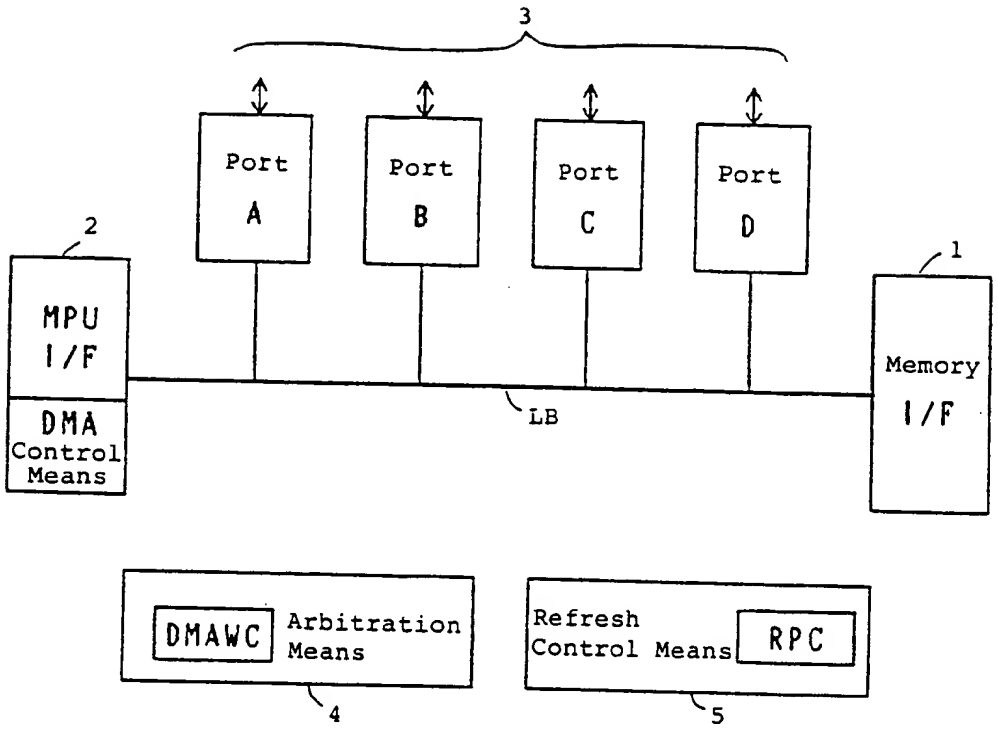


FIGURE 2

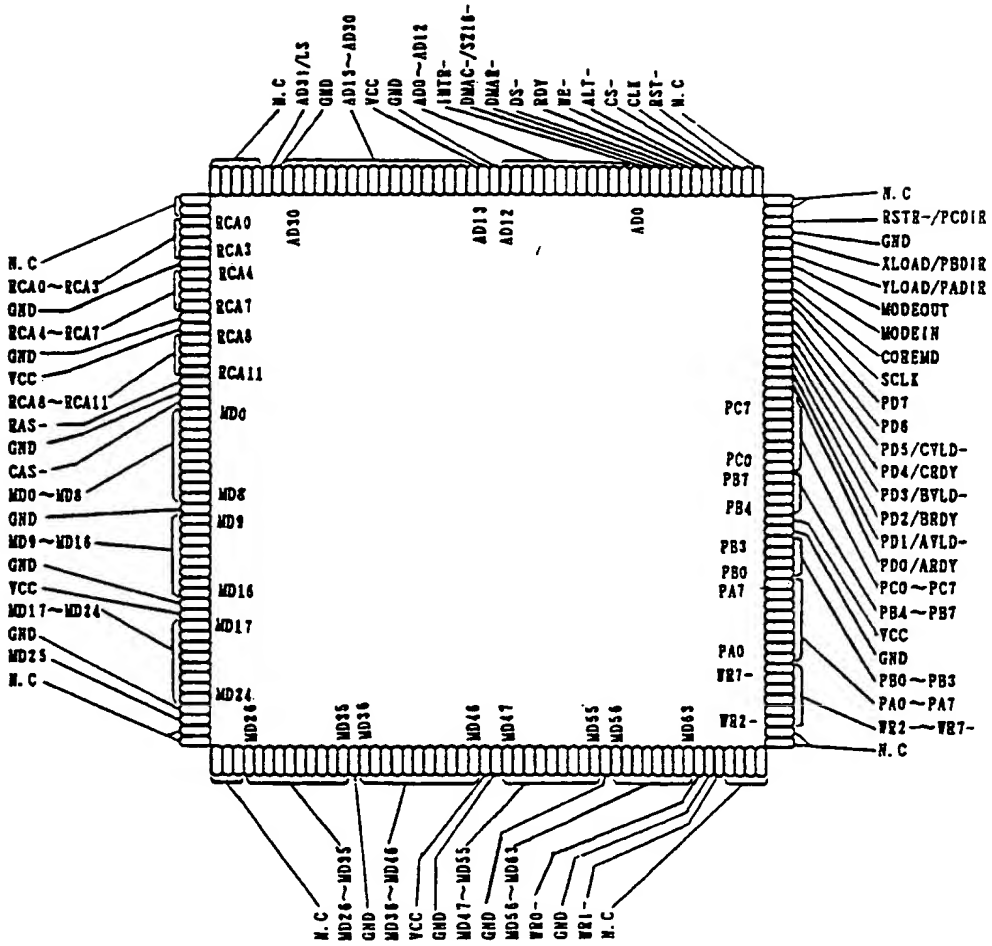


FIGURE 3

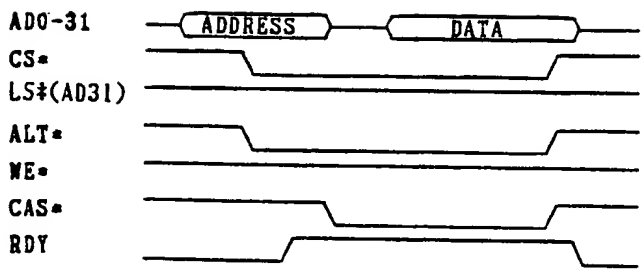


FIGURE 4

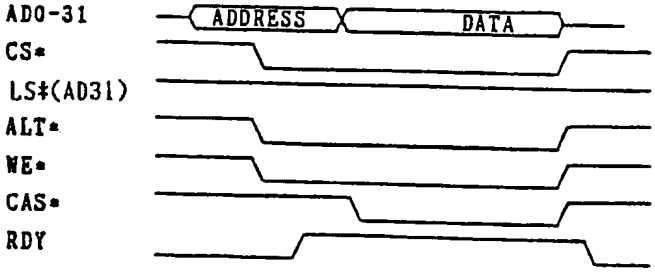


FIGURE 5

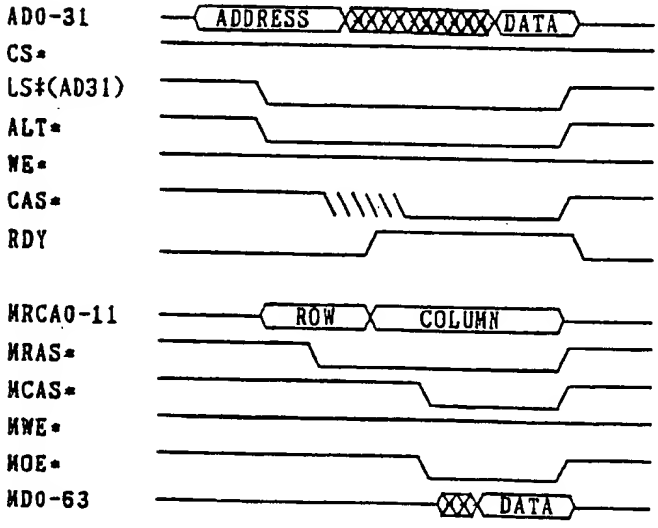


FIGURE 6

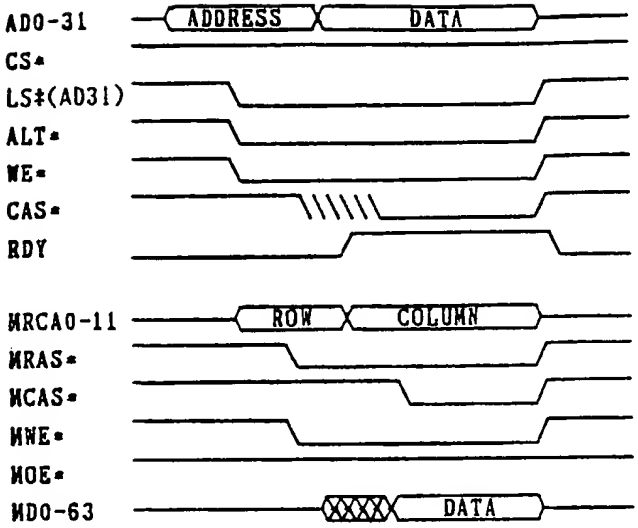


FIGURE 7

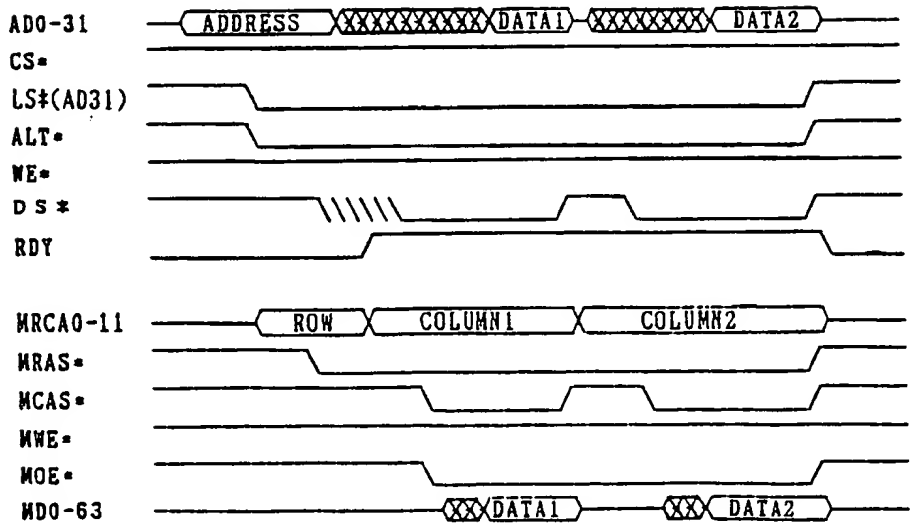


FIGURE 8

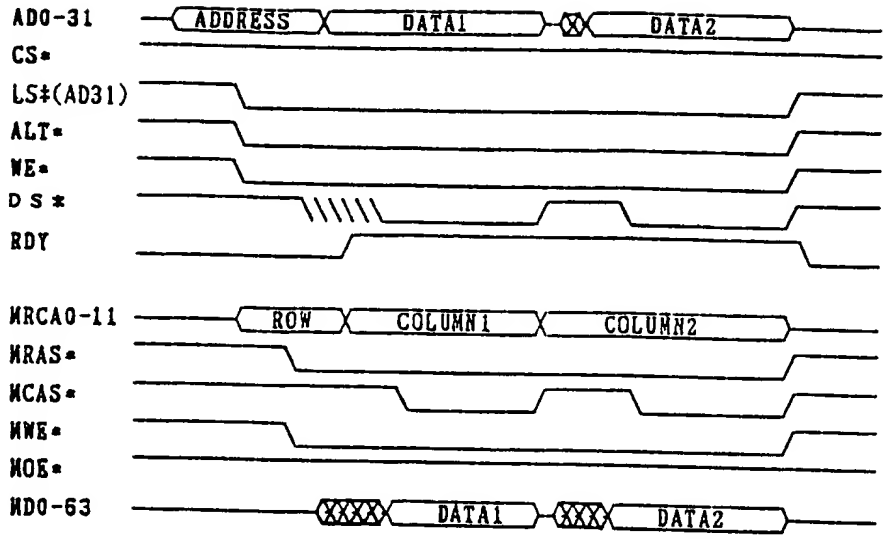


FIGURE 9

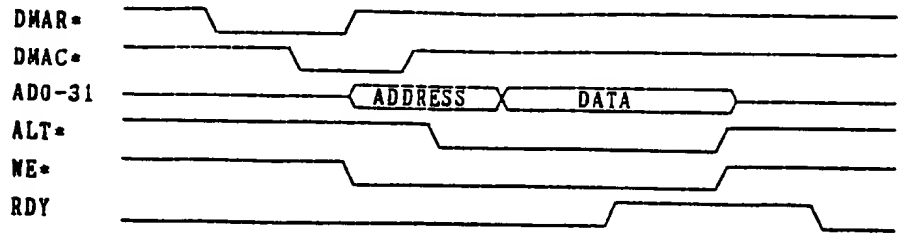


FIGURE 10

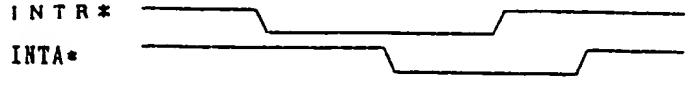


FIGURE 11

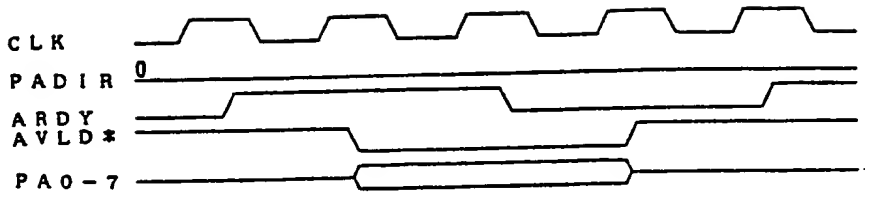


FIGURE 12

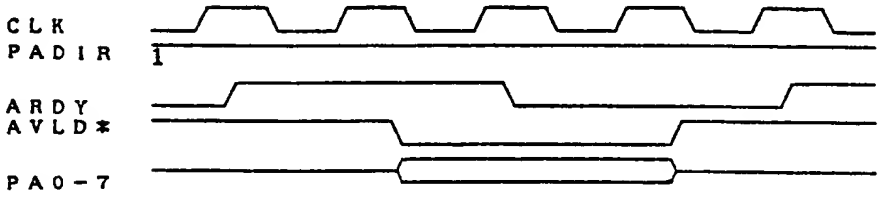


FIGURE 13

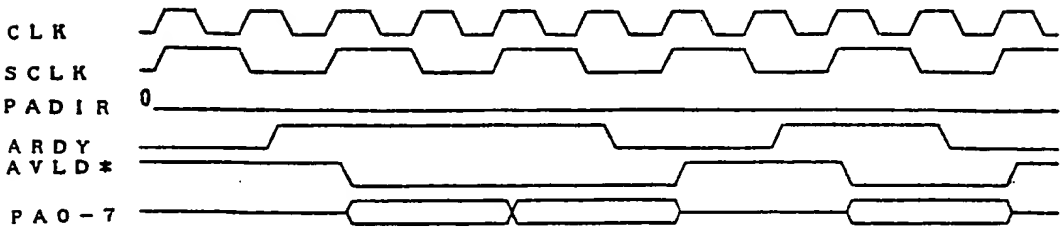


FIGURE 14

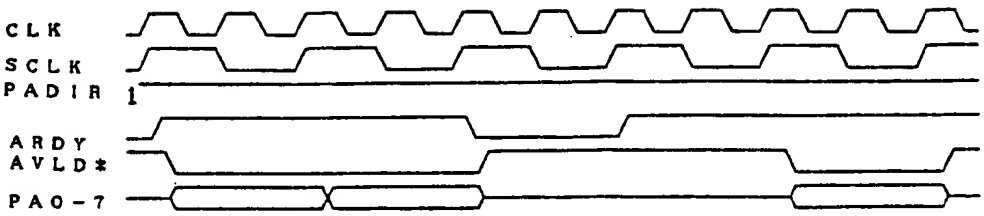


FIGURE 15

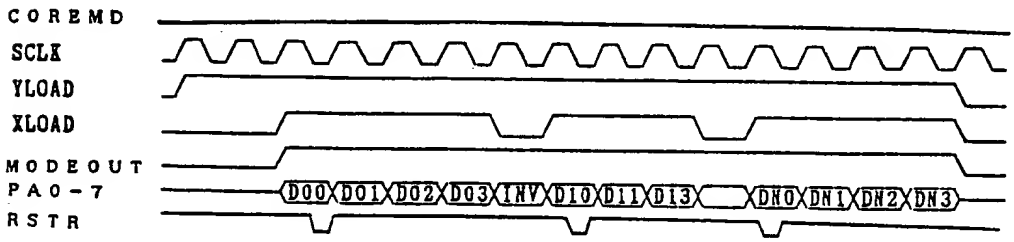


FIGURE 16

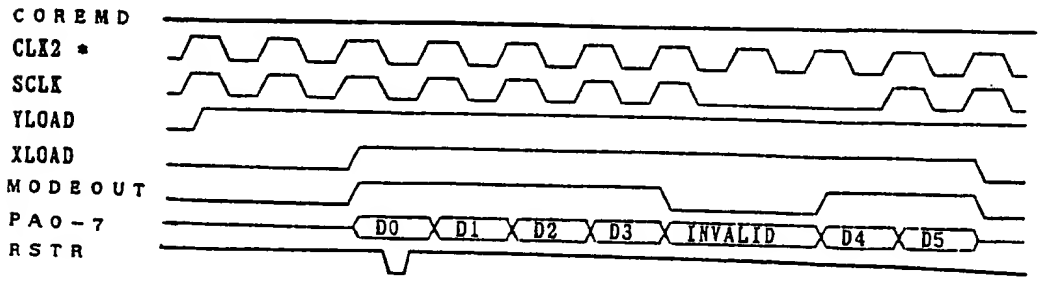


FIGURE 17

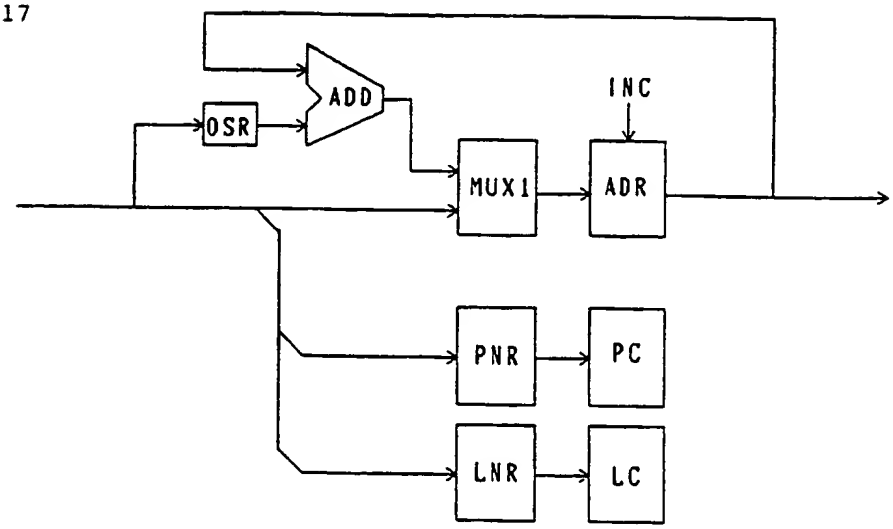


FIGURE 18

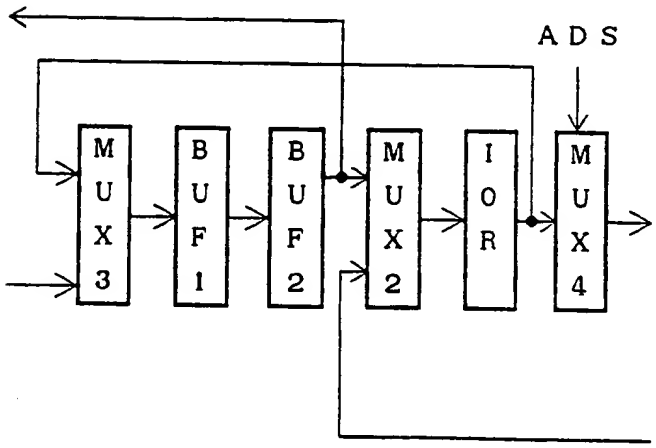
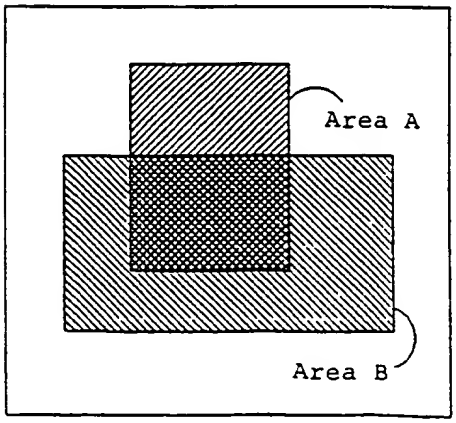


FIGURE 19



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 92 11 2950

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	EP-A-0 322 065 (LABORATOIRES D'ELECTRONIQUE PHILIPS) * page 1, line 33 - line 53 * * page 5, line 28 - line 40; figures 1,2 *	1-3	G06F13/16
X	ELECTRONIC DESIGN vol. 34, no. 22, September 1986, HASBROUCK HEIGHTS, NEW JERSEY US pages 138 - 141 , XP211515 SIDDIQUE '100-MHZ DRAM CONTROLLER SPARKS MULTIPROCESSOR DESIGNS' * page 138, left column, line 11 - line 25 * * page 138, right column, line 5 - line 18; figures 1,3 *	1,3	
X	1990 MILITARY COMMUNICATIONS CONFERENCE 3 October 1990, MONTEREY, CA, USA pages 254 - 257 , XP221792 REINER ET AL. 'VLSI DEVELOPMENT OF A GLOBAL MEMORY INTERFACE CONTROLLER' * page 254, right column *	1	TECHNICAL FIELDS SEARCHED (Int. Cl.5)
A	ELECTRONIC DESIGN vol. 35, no. 10, 30 April 1987, HASBROUCK HEIGHTS, NEW JERSEY US pages 53 - 54 BURSKY 'TRIPLE-PORT DRAM FUELS GRAPHIC DISPLAYS' * the whole document *	1-7	G06F G11C G09G
A	GB-A-2 202 978 (APPLE COMPUTER INC.) * page 2, column 1, line 1 - line 24 * * page 9, line 10 - page 12, line 23; figures 1,3,4 *	1-7	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	23 SEPTEMBER 1992	NYGREN P.P.

EPO FORM 1503 03.82 (P0401)

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document